A Half-Micron Gate Low Noise GaAs MESFET and Amplifiers

Hiroshi Kodera, Yoichi Kaneko and Hitoshi Sato
Central Research Laboratory, Hitachi, Ltd.
Kokubunji, Tokyo 185, Japan

Abstract

A half-micron gate GaAs MESFET is designed and fabricated for the minimum gate parasitics. The single bonding-pad design of the gate and intentional side-etching of the lower layer of the double-layered Schottky-gate satisfy the above requirement. The best noise figure so far measured is 2.5 dB at 10 GHz for the packaged device and 2.1 dB at 12 GHz for the chip device. An X-band unit amplifier is designed for the FET chip. It can be cascaded to get a specified power gain or modified to have a necessary bandwidth.

Introduction

The progress of GaAs MESFET's has pushed up the frequency range of three terminal devices up above Ku-band. Superior high frequency performances could not be realized without minimizing various parasitics. A half-micron gate GaAs MESFET is designed for the minimum gate parasitics and fabricated by using the chemical dry etching.

A unit amplifier is designed for the half-micron gate FET chips which is featured for the versatile applications. Addition of a simple tuning element increases the bandwidth and unit amplifiers are directly cascaded to get a specified power gain.

Design and Fabrication of GaAs FET's

Although the primary importance is put on the gate length, various parasitics have fatal effects on the high frequency performance of the GaAs FET. The high frequency performance of a GaAs FET is described by the equivalent circuit of Fig. 1. The intrinsic FET and the elements are determined from the gate length and material properties of the channel.

The parasitic resistances R_s and R_d come from the contact resistance and sheet resistance of the epitaxial layer. The parasitic capacitances C_{ge} and C_{ds} are due to the bonding pads of source and drain. Our design of the half-micron gate GaAs FET has put emphasis on the gate parasitics, R_g and C_{ges}. The metallization resistance of the gate gives rise to R_g. The larger number of gate bonding pads to reduce R_g will increase the parasitic capacitance C_{ges} between the gate and source electrodes. The noise figure will be degraded as shown in Fig. 2 with the increase of C_{ges}.

A single-pad design was adopted for the gate which was located at the center of the gate electrode and on the opposite side of the drain with source electrode in-between. In order to avoid the increase of the gate metallization resistance, a half-micron Mo Schottky barrier gate was covered with a top wider layer of Au as shown in Fig. 3. Vapor phase epitaxial crystal of n^+-n-p^- (buffer layer) structure was grown and the Schottky barrier gate was made in the moat formed by the selective etching of the n^+ layer. The gate electrode was delineated by the dry etching, where the Au layer was ion-milled with 1 μm photoresist as a mask, then a chemical etching of Mo by a CF_4 gas plasma formed a half-micron gate through the side etching[1]. The controllability of the dry etching was good to reduce the gate length down to 0.1 um.

Performance of GaAs FET's

Figure 4 shows the maximum stable gain/maximum available gain (MSG/MAG), unilateral power gain (U) and minimum noise figure (F_{min}) for a GaAs FET sealed in a ceramic disk package of 1.8 mm in diameter. The maximum frequency of oscillation, f_{max} is 90 GHz with MAG of 14 dB and the noise figure of 2.9 dB at 10 GHz.

The best noise figure of 2.48 dB was measured at 10 GHz for the packaged device. The associated gain for the best noise figure was 6.0 dB, which corresponds to the cascaded noise figure (M+1) of 3 dB at 10 GHz. The associated gain of a bare chip exceeded 10 dB with an equivalent noise figure at 10 GHz.

An alternative method to make a half-micron gate GaAs FET similar to Fig. 3 is to replace Mo by Ti and plasma etching by wet chemical etching. The use of higher doping density was attempted for the n-layer in order to improve the transconductance and to reduce the parasitic resistance. The chip device showed the best noise figure of 2.1 dB at 12 GHz with 7.6 dB associated gain as shown in Fig. 5. by an admittance Smith chart. When matched to the gain optimum condition, the power gain was increased to 10.3 dB with 3.6 dB associated noise figure.

The frequency dependence of S-parameters were fitted to the calculated parameters for the equivalent circuit of Fig. 1. The best fit was obtained for the gate resistance of 3 ohms and gate parasitic capacitance C_{ges} of 0.04 pF. Those expected from the design were 2 ohms and 0.05pF respectively.

Several reliability studies have been carried out which include operation life, high temperature storage, high temperature operation, humidity, thermal shock, temperature cycling and so on. Similar to other published work[3], source and drain electrodes degraded at elevated temperatures. The deterioration of the noise figure was correlated to the increase in the source-to-drain resistance. By adopting a criterion of 0.5 dB degradation for the noise figure, the life time of the half-micron gate GaAs FET is expected as 10^8 hours at the junction temperature of 80°C.

Low Noise Amplifiers

A Typical chip of the half-micron gate GaAs FET was characterized in a tests mount. Low noise amplifiers were designed in J- and X-band by using the equivalent circuit determined from the measured S-parameters. It was designed as a unit amplifier with input and output matched to 50 ohm line for the versatile applications. A single chip of GaAs FET is used in a circuit.

Figure 6 shows the circuit for a unit amplifire in which a quarter wavelength transformer is put in the input and output stages for the matching to the 50 ohm line. The power gain, noise figure and VSWR of a 7GHz amplifier are plotted against frequency in Fig. 7. The noise figure is 4.0 dB with the power gain around 8 dB.

The same design was applied to 12 GHz amplifier. Under the noise optimum bias condition of I_{DS}=10 mA, the noise figure was 4.8 dB which was 1.0 to 1.5 dB worse than the noise figure of a typical GaAs FET chip measured under the condition of noise optimum bias and gain optimum tuning. The power gain was 6 dB with 1 dB bandwidth of 600 MHz. Two amplifiers were cascaded to get 12 dB gain. This amplifier chain showed the noise figure of 5.5 dB and the 1 dB-bandwidth of 500 MHz.

A simple tuning element as shown by dotted lined in Fig. 6 was added to the 12 GHz amplifier to have a broader bandwidth of 4 GHz, that is 8-12 GHz amplifier. The noise figure of 5.7 dB and the power gain of 5.8 dB were observed as shown in Fig. 8.

Initial drift of the amplifier after switch-on did not exceed 1 minute. Any variation of the performance was no longer observed after that.

Conclusion

A half-micron gate GaAs MESFET was designed for the minimum gate parasitics and fabricated using an intentional side etching of the lower layer of the double-layerd Schottky gate. The packaged device showed the noise figure of 2.48 dB at 10 GHz with the corresponding cascaded noise figure of 3.0 dB. The best noise figure of the chip device was 2.1 dB at 12 GHz with the cascaded noise figure of 2.4 dB.

Low noise amplifiers were designed for the half-micron gate GaAs FET chip which are featured for the design as a unit amplifier of versatile applications. A 7GHz amplifier showed the noise figure of 4.0 dB and a 12 GHz amplifier showed the noise figure of 4.8 dB. Addition of a simple tuning element widened the bandwidth to 4 GHz.

Acknowledgement

The authors wish to express thanks to Messrs. M. Hirano, H. Kurono, S. Takahashi and F. Murai for their cooperation during the work.

References

1) S. Takahashi, F. Murai, H. Kurono, M. Hirao and H. Kodera, "A Half-Micron Gate GaAs FET fabricated by Chemical Dry Etching", Digest of Technical Papers, The 8th Conf. (1976 International) Solid State Devices, Tokyo, 1976, pp. 41-42, September 1976.

2) S. Takahashi, F. Murai, S. Asai and H. Kodera, "Reproducible Submicron Gate Fabrication of GaAs FET by plasma Etching", Digest of Technical Papers, Intern. Electron Devices Meeting, Washington, 1976, pp. 214-217, December, 1976.

3) T. Irie, I. Nagasako, H. Kohzu and K. Sekido, "Reliability Study of GaAs MESFET's", IEEE Trans. Microwave Theory and Technique, vol. MTT-24, pp. 321-328, June, 1976.

Figure Captions

Fig. 1. Equivalent Circuit of a GaAs FET. (Package parasitics are omitted.)

Fig. 2. Effect of the gate parasitic capacitance on the noise figure analyzed from the equivalent circuit of a GaAs FET.

Fig. 3. Planar and cross sectional structure of the half-micron gate GaAs FET.
(A) Planar view
(B) Cross sectional view along A-A'

Fig. 4. Power gain and noise figure of a half-micron gate GaAs FET.

Fig. 5. Admittance Smith chart for the optimum noise and gain of a half-micron gate GaAs FET chip.

Fig. 6. The circuit diagram of a unit amplifier.

Fig. 7. Performance of a 7 GHz amplifier.

Fig. 8. A broad band 8-12 GHz amplifier modified from a unit amplifier design.

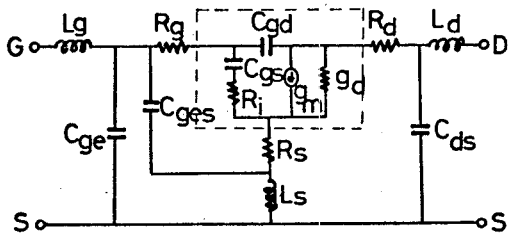


Fig. 1. Equivalent Circuit of a GaAs FET. (Package parasitics are omitted.)

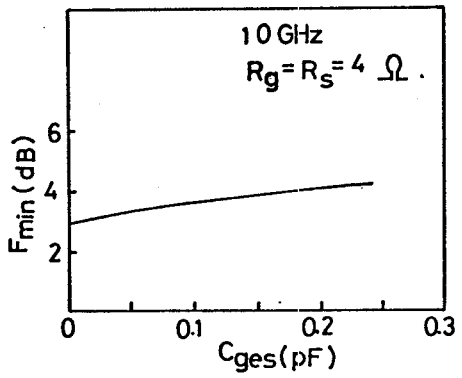
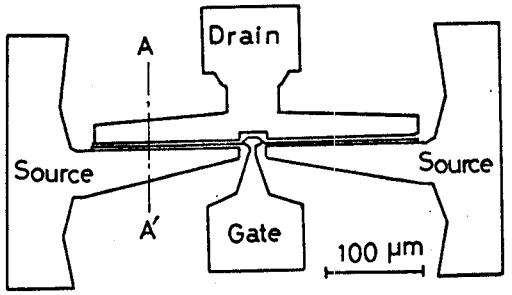
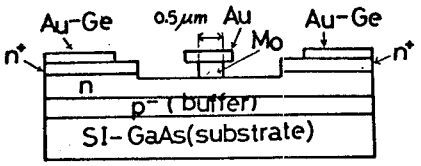


Fig. 2. Effect of the gate parasitic capacitance on the noise figure analyzed from the equivalent circuit of a GaAs FET.



(A)



(B)

Fig. 3. Planar and cross sectional structure of the half-micron gate GaAs FET.
(A) Planar view
(B) Cross sectional view along A-A'

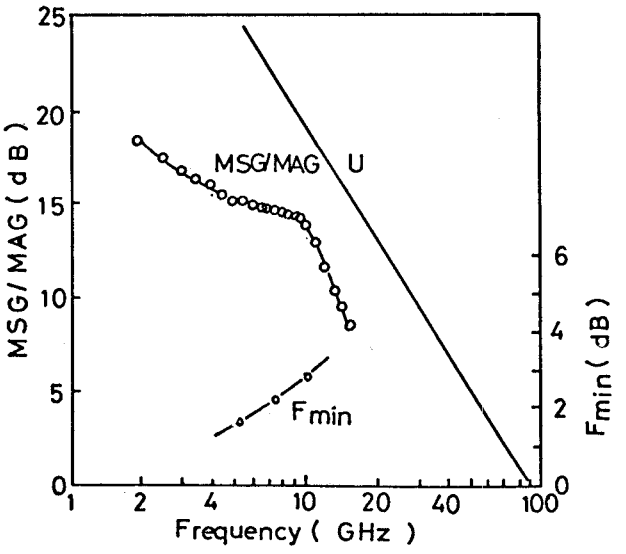


Fig. 4. Power gain and noise figure of a half-micron gate GaAs FET.

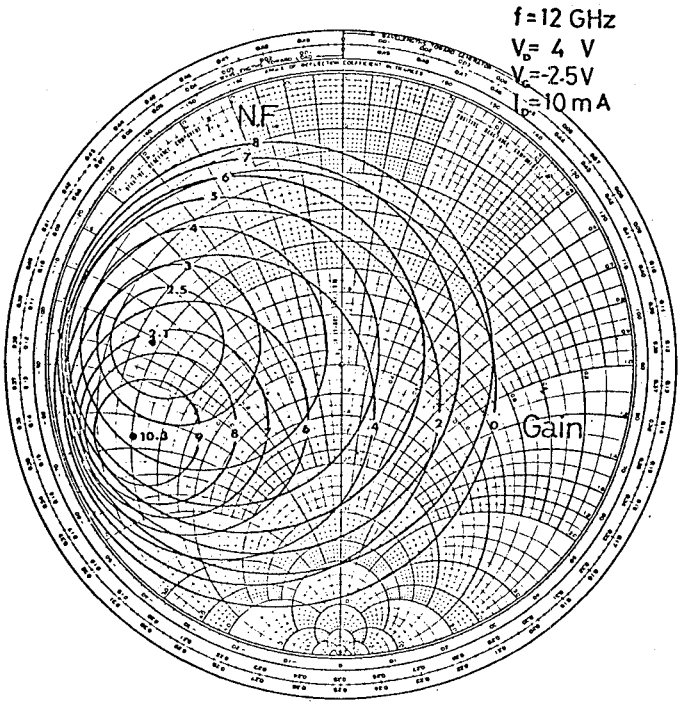


Fig. 5. Admittance Smith chart for the optimum noise and gain of a half-micron gate GaAs FET chip.

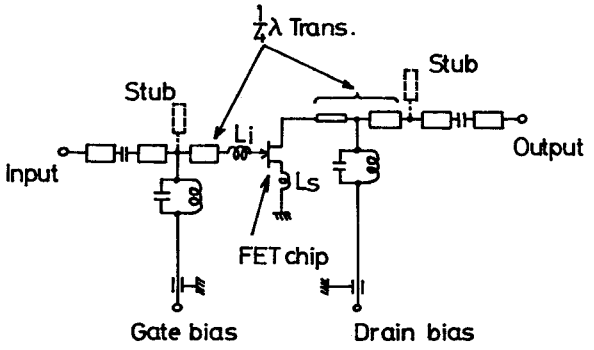


Fig. 6. The circuit diagram of a unit amplifier.

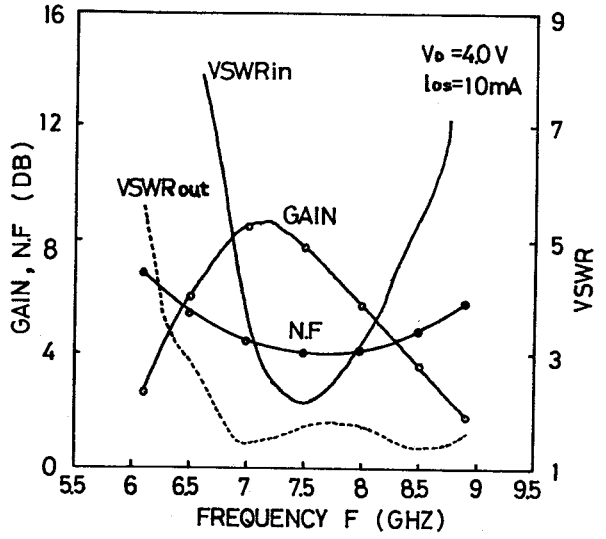


Fig. 7. Performance of a 7 GHz amplifier.

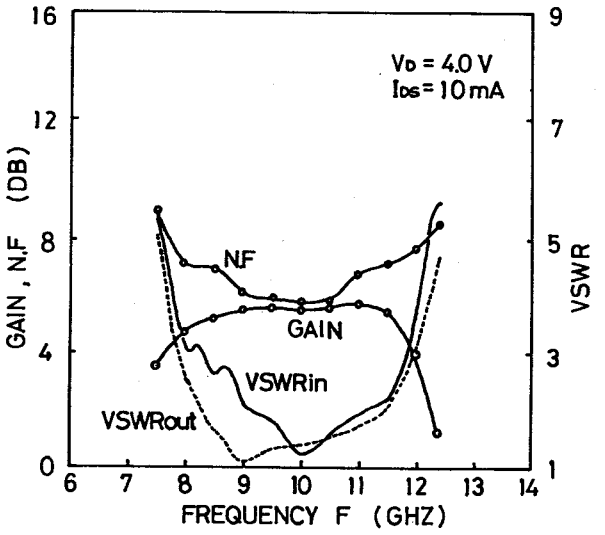


Fig. 8. A broad band 8-12 GHz amplifier modified from a unit amplifier design.